CLAIMS

What is claimed is:

1. A system comprising:

first and second modules;

a circuit board including first and second module connectors to receive the first and second modules, respectively;

a first path of conductors extending from the circuit board to the first module connector, to the first module, back to the first module connector, to the circuit board, to the second module connector, to the second module, and to on module terminations of the second module; and

a second path of conductors extending from the circuit board to the second module connector, to the second module, back to the second module connector, to the circuit board, to the first module connector, to the first module, and to on module terminations of the first module.

2. The system of claim 1, wherein the first and second module connectors each have front sides and back sides, and the first path extends from the back side of the first module to the back side of the second module.

3. The system of claim 1, wherein the first and second module connectors each have front sides and back sides, and the first path extends from the back side of the first module to the front side of the second module.

4. The system of claim 1, wherein the first and second modules and first and second module connectors are keyed so the first and second modules each may be received in only one rotational orientation.

5. The system of claim 1, wherein the first and second modules are interchangeable so that the first module may be received by the second module connector and the second module received by the first module connector without rotating the orientation of either module.

6. The system of claim 1, wherein the system includes X paths including the first and second paths, and the first and second modules each include 2X chips and wherein each of the X paths couples to stubs for a different two of the 2X chips of the first module and for a different two of the 2X chips of the second module.

7. The system of claim 1, further comprising a buffer on the first module and a buffer on the second module.

8. The system of claim 1, further comprising error correction code chips on the first module and error correction code chips on the second module.

9. The system of claim 8, wherein the error correction code chips are terminated on the circuit board.

10. The system of claim 1, wherein:

a first section of the first path, which is a short loop through section, couples to stubs for only first and second chips of the first module, and a second section of the first path couples to stubs for only first and second chips of the second module; and

a first section of the second path, which is a short loop through section, couples to stubs for only third and fourth chips of the second module and a section of the second path couples to stubs for only third and fourth chips of the first module.

11. The system of claim 1, wherein:

a first section of the first path, which is a short loop through section, couples to stubs for only one chip of the first module, and a second section of the first path couples to stubs for only one chip of the second module; and

a first section of the second path, which is a short loop through section, couples to stubs for only one chip of the second module and a section of the second path couples to stubs for a only one chip of the first module.

12. The system of claim 1, further comprising a controller coupled to the first and second paths.

13. The system of claim 1, wherein the circuit board is a printed circuit board and a motherboard.

14. The system of claim 1, wherein impedances of the paths in the modules is at least 50% higher than the paths on the circuit boards.

15. The system of claim 1, wherein there are additional paths having a path like that of the first path and other additional paths having a path like that of the second path.

16. A system comprising:

a circuit board including first and second module connectors each including module slots;

a first path of conductors extending from the circuit board to the first module connector to a first group of module connector contacts of the first module connector, extending from a second group of module connector contacts of the first module connector to the circuit board, to the second module connector, to a first group of module connector contacts on the second module connector, there being a gap between the first and second groups of module connector contacts of the first module connector;

a second path of conductors extending from the circuit board to the second module connector to a first group of module connector contacts of the second module connector, extending from a second group of module connector contacts of the second module connector to the circuit board, to the first module connector, to a first group of module connector contacts on the first module connector, there being a gap between the first and second groups of module connector contacts of the second module connector.

17. The system of claim 16, wherein there are module connector connections between the circuit board and the first and second module connectors on the path.

18. The system of claim 16, wherein there are additional paths having a path like that of the first path and other additional paths having a path like that of the second path.

19. The system of claim 16, wherein there are module connector connections between the circuit board and the first and second module connectors on the path.

20. The system of claim 16, wherein the first and second module connectors are keyed such that a similarly keyed module can be inserted in only one orientation into the corresponding module slot.

21. A system comprising:

first and second modules;

a circuit board including first and second module connectors to receive the first and second modules, respectively;

a first path of conductors extending from the circuit board to the first module connector, to the first module, back to the first module connector, to the circuit board, to the second module connector, to the second module, to an on module termination of the second module, wherein a

first section of the first path, which is a short loop through section, couples to stubs for first and second chips of the first module, and a second section of the first path couples to stubs for first and second chips of the second module; and

a second path of conductors extending from the circuit board to the second module connector, to the second module, back to the second module connector, to the circuit board, to the first module connector, to the first module, to an on module termination of the first module, wherein a first section of the second path, which is a short loop through section, couples to stubs for third and fourth chips of the second module and a section of the second path couples to stubs for third and fourth chips of the first module.

22. The system of claim 21, wherein the system includes

X paths including the first and second paths, and

the first and second modules each include 2X chips including the first, second, third, and fourth chips of the first and second modules, and wherein each of the X paths couples to stubs for a different two of the 2X chips of the first module and for a different two of the 2X chips of the second module.

23. The system of claim 21, wherein the first and second module connectors each have front sides and back sides, and the first path extends from the back side of the first module to the back side of the second module.

24. The system of claim 21, wherein the first and second module connectors each have front sides and back sides, and the first path extends from the back side of the first module to the front side of the second module.

25. The system of claim 21, wherein the first and second modules and first and second module connectors are keyed so as to be able to be received by the modules in only one orientation.

26. The system of claim 21, wherein the first and second modules are interchangeable so that the first module may be received by the second module connector and the second module received by the first module connector without rotating the orientation of either module.

27. The system of claim 21, further comprising a buffer on the first module and a buffer on the second module.

28. The system of claim 21, further comprising error correction code chips on the first module and error correction code chips on the second module.

29. The system of claim 21, wherein there are additional paths having a path like that of the first path and other additional paths having a path like that of the second path.